AMENDMENTS TO THE CLAIMS

Claims 1-10. (canceled)

11. (currently amended) A semiconductor device comprising:

a substrate; and

at least two non-overlapping gate structures formed in a single layer on said substrate, said gate structures being spaced apart by a gap measuring less than 1300 Angstroms, wherein at least one of the gate structures is a transistor gate structure.

12. (previously presented) The semiconductor device according to claim 11, wherein said gap measures no less than approximately 300 Angstroms.

13. (original) The semiconductor device according to claim 11, wherein the at least two gate structures are formed of a conductive material selected from polysilicon, silicide, metal, polysilicon and silicide, and polysilicon and metal.

14. (original) The semiconductor device according to claim 11, wherein the gate structures are transistor gates in a CCD imager.

15. (original) The semiconductor device according to claim 11, wherein the gate structures are transistor gates in a CMOS imager.

16. (original) The semiconductor device according to claim 15, wherein the CMOS imager has one of a 3T, 4T, 5T, 6T or 7T architecture.

17. (currently amended) The semiconductor device according to claim 15, wherein the transistor gates include at least two of ~~a photogate,~~ a transfer gate, a reset gate, a source follower gate, a row select gate, and a storage gate.

18. (original) The semiconductor device according to claim 11, further comprising a lightly doped region between two adjacent ones of the gate structures.

19. (original) The semiconductor device according to claim 18, wherein the lightly doped region is implanted with ions in the range of about $3 \cdot 10^{11}$ ions/ cm^2 to about $1 \cdot 10^{14}$ ions/ cm^2.

20. (original) The semiconductor device according to claim 19, wherein the lightly doped region is implanted with ions in the range of about $1 \cdot 10^{12}$ ions/ cm^2 to about $1 \cdot 10^{13}$ ions/ cm^2.

21. (original) The semiconductor device according to claim 18, wherein the at least two gate structures are transistor gates for a CCD imager.

22. (currently amended) The semiconductor device according to claim 18, wherein the at least two gate structures are transistor gates for a CMOS imager and the two adjacent gate structures having the lightly doped region therebetween are selected from among ~~a photogate,~~ a transfer gate, a reset gate, a source follower gate, a row select gate and a storage gate.

23. (currently amended) The semiconductor device according to claim 22, wherein the two adjacent gate structures having the lightly doped region therebetween include ~~a photogate and either~~ a transfer gate or a storage gate.

24. (original) The semiconductor device according to claim 22, wherein the two adjacent gate structures having the lightly doped region therebetween are n-channel gates and the lightly doped region therebetween is an n-type region.

25. (original) The semiconductor device according to claim 22, wherein the two adjacent gate structures having the lightly doped region therebetween are p-channel gates and the lightly doped region therebetween is a p-type region.

26. (currently amended) A semiconductor device comprising:

a substrate;

a plurality of non-overlapping conductive gates formed over the substrate; and

a lightly doped region in the substrate between two adjacent ones of the plurality of conductive gates, the two adjacent ones of the plurality of conductive gates being formed in a single layer and separated by a gap of less than 1300 Angstroms, wherein at least one of the two adjacent ones of the plurality of gates is a transistor gate.

27. (original) The semiconductor device according to claim 26, wherein the lightly doped region is implanted with ions in the range of about $3 \cdot 10^{11}$ ions/ cm^2 to about $1 \cdot 10^{14}$ ions/ cm^2.

28. (original) The semiconductor device according to claim 27, wherein the lightly doped region is implanted with ions in the range of about $1 \cdot 10^{12}$ ions/ cm^2 to about $1 \cdot 10^{13}$ ions/ cm^2.

29. (currently amended) The semiconductor device according to claim 26, wherein the plurality of conductive gates ~~are~~ includes transistor gates for a CCD imager.

30. (currently amended) The semiconductor device according to claim 26, wherein the plurality of conductive gates ~~are~~ includes transistor gates for a CMOS imager and the two adjacent conductive gates having the lightly doped region therebetween are selected from among a photogate, a transfer gate, a reset gate, a source follower gate, a row select gate and a storage gate.

31. (original) The semiconductor device according to claim 30, wherein the two adjacent conductive gates having the lightly doped region therebetween include a photogate and either a transfer gate or a storage gate.

32. (original) The semiconductor device according to claim 30, wherein the two adjacent conductive gates having the lightly doped region therebetween are n-channel gates and the lightly doped region is an n-type region.

33. (currently amended) The semiconductor device according to claim 30, wherein the two adjacent conductive gates having the lightly doped region therebetween are p-channel gates and the lightly doped region is ~~an~~ a p-type region.

34. (currently amended) An image processing apparatus comprising:

an image sensor for detecting an image and outputting image signals corresponding to the detected image; and

an image processor for processing the image signals outputted from the image sensor,

wherein the image sensor comprises:

a substrate; and

at least two non-overlapping gate structures formed in a single layer on said substrate, said gate structures being spaced apart by a gap measuring less than 1300 Angstroms, wherein at least one of the gates structures is a transistor gate.

35. (previously presented) The image processing apparatus according to claim 34, said gap measuring no less than approximately 300 Angstroms.

36. (original) The image processing apparatus according to claim 34, wherein the image sensor is a CCD image sensor.

37. (original) The image processing apparatus according to claim 34, wherein the image sensor is a CMOS image sensor.

38. (original) The image processing apparatus according to claim 34, further comprising a lightly doped region between two of the gate structures.

39. (previously presented) An image processing apparatus comprising:

an image sensor for detecting an image and outputting image signals corresponding to the detected image; and

an image processor for processing the image signals outputted from the image sensor,

wherein the image sensor comprises:

a substrate;

a plurality of conductive gates formed over the substrate; and

a lightly doped region in the substrate between at least one pair of adjacent non-overlapping conductive gates formed in a single layer and separated by a gap of less than 1300 micrometers.

40. (currently amended) A processing system, comprising:

a processor for receiving and processing image data; and

an image data generator for supplying image data to the processor, the image data generator comprising

an image sensor for obtaining an image and outputting an image signal,

an image processor for processing the image signal, and

a controller for controlling the image sensor and the image processor,

wherein the image sensor comprises:

a substrate, and

at least two non-overlapping gate structures formed in a single layer on said substrate, said gate structures being spaced apart by a gap measuring less than 1300 Angstroms, wherein at least one of the gate structures is a transistor gate.

41. (original) The processing system according to claim 40, wherein the image sensor is a CCD imager.

42. (original) The processing system according to claim 40, wherein the image sensor is a CMOS imager.

43. (original) The processing system according to claim 40, further comprising a lightly doped region between at least one pair of adjacent gate structures.

44. (previously presented) A processing system, comprising:

a processor for receiving and processing image data; and

an image data generator for supplying image data to the processor, the image data generator comprising

an image sensor for obtaining an image and outputting an image signal,

an image processor for processing the image signal, and

a controller for controlling the image sensor and the image processor,

wherein the image sensor comprises:

a substrate;

a plurality of non-overlapping conductive gates formed over the substrate; and

a lightly doped region in the substrate between two adjacent ones of the plurality of conductive gates, the adjacent conductive gates being formed in a single layer and separated by a gap of less than 1300 Angstroms.